We claim:

- 1. A method to improve the threshold voltage (Vt) roll-off in an NMOS transistor that includes a shallow trench isolation feature, comprising:
 - (a) providing a substrate having an active area where an NMOS transistor will be built;
 - (b) forming trenches in said substrate wherein the shallow trenches separate active areas in said substrate;
 - (c) forming a liner on the surface of said substrate and on the sidewalls and bottom of said shallow trenches;
 - (d) forming a plug in said shallow trenches; said plug is recessed below the top of said substrate;
 - (e) performing an angled indium implant through said shallow trenches into the substrate adjacent to top corners of the trenches;
 - (f) removing said plug and depositing an insulator layer to fill said shallow trenches;
 - (g) planarizing said insulator layer; and
 - (h) forming a gate dielectric layer on said substrate and forming a patterned gate layer over said gate dielectric layer and over said insulator layer.
- 2. The method of claim 1 wherein said shallow trenches are formed by depositing a pad oxide on said substrate, depositing a cap layer on said pad oxide, patterning a photoresist on said cap layer and transferring trench openings in said photoresist into said substrate with a plasma etch process.
 - 3. The method of claim 2 wherein said cap layer is silicon nitride.

- 4. The method of claim 1 wherein said shallow trenches have a width in the range of less than 100 nm to several microns and a depth into said substrate between about 1500 and 5000 Angstroms and wherein said active areas have a width that ranges from less than 100 nm to several microns.
- 5. The method of claim 1 wherein said liner is a layer of thermal oxide having a thickness from about 30 to 500 Angstroms.
- 6. The method of claim 1 wherein said plug is formed by coating a photoresist or polymer layer on said substrate and then etching back said photoresist or polymer layer.
- 7. The method of claim 1 wherein the top of said recessed plug is a distance about 300 to 1700 Angstroms below the top of said substrate.
- 8. The method of claim 1 wherein said angled indium implant is performed with an energy between about 10 and 300 keV at an angle of about 0^o to 60^o and with a dose in the range of about 1e12 to 5e13 ions/cm².
- 9. The method of claim **8** wherein said implant forms doped regions in said substrate adjacent to said shallow trenches having a thickness between about 30 and 1000 Angstroms and with an indium concentration from about 10¹⁴ to 10¹⁹ ions/cm³.
- 10. The method of claim 8 wherein said implant forms a doped region in said substrate that extends away from a shallow trench by a distance of 0 to about 1000 Angstroms.
- 11. The method of claim 1 wherein the insulator layer is comprised of SiO₂ or a low k dielectric material.
- 12. The method of claim 1 wherein said gate dielectric layer is comprised of SiO₂ or is comprised of an upper high k dielectric metal oxide layer on a lower interfacial layer.

- 13. The method of claim **2** further comprised of removing said pad oxide and cap layers prior to formation of said gate dielectric layer.
- 14. A method to improve the threshold voltage (Vt) roll-off in an NMOS transistor by fabricating a shallow trench isolation structure, comprising:
 - (a) providing a substrate having an active area where an NMOS transistor will be built;
 - (b) forming shallow trenches in said substrate; said shallow trenches separate active areas in said substrate;
 - (c) growing an oxide liner layer on the sidewalls and bottom of said shallow trenches;
 - (d) forming a plug in said shallow trenches wherein said plug is recessed below the top of said substrate;
 - (e) performing an angled indium implant through said trench openings into the substrate adjacent to top corners of the shallow trenches;
 - (f) removing said plug layer; and
 - (g) depositing an insulator layer in said shallow trenches and planarizing said insulator layer.
- 15. The method of claim **14** wherein said shallow trenches are formed by depositing a pad oxide on said substrate and a silicon nitride cap layer on said pad oxide followed by patterning a photoresist on said nitride layer and transferring openings in said patterned photoresist into said substrate with a plasma etch process.

- 16. The method of claim **15** further comprised of removing said pad oxide and nitride layers following said planarization step, depositing a gate dielectric layer on said active areas and patterning a gate layer on said gate dielectric layer.
- 17. The method of claim **14** wherein said shallow trenches have a width in the range of less than 100 nm to several microns and a depth into said substrate between about 1500 and 5000 Angstroms.
- 18. The method of claim **14** wherein said oxide liner has a thickness from about 30 to 500 Angstroms.
- 19. The method of claim **14** wherein said recessed plug is formed by coating a photoresist or polymer layer on said substrate and then etching back said photoresist or polymer layer.
- 20. The method of claim **14** wherein the top of said recessed plug is a distance about 300 to 1700 Angstroms below the top of said substrate.
- 21. The method of claim **14** wherein said angled indium implant is performed with an energy between about 10 and 300 keV at an angle of 0^o to about 60^o and with a dose in the range of about 1e12 to 5e13 ions/cm².
- 22. The method of claim **21** wherein said implant forms doped regions in said substrate adjacent to said shallow trenches; said doped regions have a thickness between about 30 and 1000 Angstroms and with an indium concentration from about 10¹⁴ to 10¹⁹ ions/cm³.
- 23. The method of claim **21** wherein said implant forms a doped region in said substrate that extends away from a shallow trench by a distance of 0 to about 1000 Angstroms.

- 24. The method of claim **14** wherein the insulator layer is comprised of SiO₂ or a low k dielectric material.
- 25. The method of claim **14** further comprised of performing an anneal step to activate the dopant in implanted regions of said substrate.
 - 26. An NMOS transistor having an improved narrow width Vt roll-off, comprising:
- (a) a substrate that includes shallow trench isolation (STI) features which are comprised of a shallow trench with sloped sidewalls and a bottom, an oxide liner formed on said shallow trench sidewalls and bottom, and an insulator layer formed on said oxide liner that fills said shallow trench and extends to a level that is above the top of said substrate;
- (b) an active area formed between two adjacent shallow trenches in said substrate; said active area having an indium doped region that is adjacent to top corners of said shallow trenches:
 - (c) a gate dielectric layer formed on said active areas; and
 - (d) a patterned gate layer formed on said gate dielectric layer wherein said gate layer extends over said adjacent shallow trenches.
- 27. The NMOS transistor of claim **26** wherein said substrate is also comprised of a second p-type dopant in said active areas;
- 28. The NMOS transistor of claim **26** wherein the depth of said shallow trench is about 1500 to 5000 Angstroms and the width of the shallow trench ranges from less than 100 nm to several microns.
- 29. The NMOS transistor of claim **26** wherein said oxide liner has a thickness of about 50 to 300 Angstroms.

- 30. The NMOS transistor of claim **26** wherein said insulator layer is comprised of SiO₂ or a low k dielectric material.
- 31. The NMOS transistor of claim **26** wherein said doped indium region has an indium concentration from about 10¹⁴ to 10¹⁹ ions/cm³ and has a thickness in the range of about 30 to 1000 Angstroms.
- 32. The NMOS transistor structure of claim **26** wherein said indium doped region extends away from said shallow trench to a distance between 0 and about 1000 Angstroms.
- 33. The structure of claim **26** wherein said gate dielectric layer is comprised of SiO₂ or an upper high k dielectric metal oxide layer on a lower interfacial layer.
- 34. The NMOS transistor of claim **26** wherein said gate layer has a thickness of about 300 to 5000 Angstroms and forms a conformal layer on said gate dielectric layer and on said adjacent STI features.
- 35. The structure of claim **26** wherein said gate layer is comprised of doped polysilicon.
- 36. The NMOS transistor of claim **26** wherein said gate layer is comprised of undoped polysilicon or amorphous silicon.